**Amendment to the Claims:**

This listing of claims will replace all versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Currently Amended) An externally non-addressable memory for outputting an executable code sequence comprising:

a plurality of data storage locations;

a plurality data lines adapted for outputting data stored in the plurality of data storage locations;

an internal address register adapted for storing address information associated with a memory location associated with an instruction to be output on the data lines;

means for switching to a sequential mode responsive to an external run signal being asserted;

means for loading a preselected address into the internal address register responsive to the means for entering a sequential mode;

counter means for sequentially incrementing the internal address register so that instructions of the code sequence sequentially appear on the data lines until completion thereof so as to be synchronous with an instruction fetch sequence of an associated processor; and

means for switching to a normal mode responsive to the external signal being negated.

2. (Original) The memory of claim 1 further comprising means for receiving an externally generated clock signal, wherein the counter means is incremented in accordance with the externally generated clock signal.

3. (Original) The memory of claim 2 further comprising means adapted for receiving the run signal from an associated data device.

4. (Currently Amended) The memory of claim 2 further comprising means for generating the run signal in accordance with a power on state of a[[n]] data processing device into which the memory is incorporated.

5. (Original) The memory of claim 1 further comprising means for generating a wait signal corresponding to a duration in which no valid data is available on the data lines.

6. (Original) The memory of claim 1 further comprising an associated, addressable, random access memory into which the code sequence is copied.

7. (Original) The memory of claim 2 further comprising an associated processor device, which processor device is synchronized so as to operate on instructions the code sequence as it is output onto the data lines.

8. (Currently Amended) A bootable NAND flash memory comprising:

a plurality of instruction storage locations;

a plurality data lines adapted for outputting instructions stored in the plurality of data storage locations;

an internal address register adapted for storing address information associated with a memory location in which is stored one of a plurality instructions associated with a boot sequence is to be output on the data lines;

means for switching to a sequential mode in accordance with a boot signal representative of a commencement of a boot code sequence;

means for loading a preselected address into the internal address register responsive to the means for switching to a sequential mode;

counter means for sequentially incrementing the internal address register so that instructions of the boot sequence sequentially appear on the data lines until completion thereof so as to be synchronous with an instruction fetch sequence of an associated processor; and

means for switching to a normal operating mode upon de-assertion of the boot signal.

9. (Original) The bootable NAND flash memory of claim 8 further comprising a boot signal generator for generating the boot signal upon power up of a data processing device.

10. (Original) The bootable NAND flash memory of claim 9 further comprising an addressable, random access memory in data communication with the data lines into which the boot sequence is copied.

11. (Original) The bootable NAND flash memory of claim 10 wherein the boot signal generator is comprised of a central processor unit.

12. (Original) The bootable NAND flash memory of claim 11 further comprising a means for generating a busy signal representative of a duration in which valid boot data is not available on the data lines.

13.-15. (Cancelled)

16. (Currently Amended) A method of running programs disposed in a non-externally addressable memory comprising the steps of:

receiving a run signal representative of a commencement of a preselected code sequence disposed in the non-externally addressable memory;

upon receipt of the run signal, switching to a sequential mode of operation and preloading an internal address register with a preselected address corresponding with a first instruction of the code sequence;

outputting an instruction associated with the address of the internal address register;

incrementing the internal address register so as to output each instruction forming the preselected code sequence synchronously with an instruction fetch sequence of an associated processor; and

switching to a normal mode of operation after each instruction forming the preselected code sequence has been output.

17. (Original) The method of claim 16 further comprising the step of synchronizing the incrementing of the internal address register to correspond with instructions receivable into an associated, central processor unit.

18. (Original) The method of claim 16 further comprising the step of copying the preselected code sequence into an associated, addressable random access memory.

19. (Original) The method of claim 18 further comprising the step of generating the run signal in accordance with at least one of power up and a reset of a data processing device.

20. (Original) The method of claim 19 further comprising the step of transferring instructions from a secondary memory device upon completion of the code sequence.

21. (Currently Amended) An externally non-addressable memory for outputting an executable code sequence comprising:

a plurality of data storage locations;

a plurality data lines adapted for outputting data stored in the plurality of data storage locations;

an internal address register storing address information associated with a memory location associated with an instruction to be output on the data lines, the internal address register receiving a preselected address upon receipt of a run signal representative of a commencement of a preselected code sequence comprised of a plurality of executable instructions stored in the plurality of data storage locations signal;

a counter to sequentially increment a content of the internal address register in response to a clock signal so that instructions of the code sequence sequentially appear on the data lines in series responsive to the run instruction synchronously with an instruction fetch sequence of an associated processor; and

means for switching to a normal mode of operation after the code sequence has been output.

22. (Original) The memory of claim 21 wherein the plurality of data storage locations include nonvolatile memory cells.

23. (Original) The memory of claim 22 wherein the run signal is generated in response to a power on state of an data processing device into which the memory is incorporated.

24. (Original) The memory of claim 21 wherein the memory receives a wait signal representing a duration in which no valid data is available on the data lines.

25. (Cancelled)